



Atty. Dkt. No. 00AB007 (081696-0234)

5/Supp  
B  
9-25-03  
NP

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Gary Dan Dotson  
Title: MINIMUM MOVE TOUCH PLANE  
SCANNING METHOD AND DEVICE  
Appl. No.: 09/675,863  
Filing Date: 09/29/2000  
Examiner: Nguyen, Kimnhung T.  
Art Unit: 2674

<b>CERTIFICATE OF MAILING</b> I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on the date below.  Karen Meier (Printed Name)  <i>Karen Meier</i> (Signature)  April 2, 2003 (Date of Deposit)
---

SUPPLEMENTAL AMENDMENT

Box **NON-FEE AMENDMENT**  
Commissioner for Patents  
Washington, D.C. 20231

RECEIVED

APR 10 2003

Technology Center 2600

Sir:

Please amend the above-identified application as follows:

**In the Drawings:**

A separate Request to Approve Drawing Changes is attached. Copies of the drawing figures showing requested change in red are submitted with this document.

**In the Specification:**

- **Delete the tenth full paragraph at page 7, lines 20-23 through page 8, lines 1-11 and substitute the following paragraph:** *(The changes are shown explicitly in the attached "Version With Markings to Show Changes Made.")*

Referring now to FIG. 2, FIG. 2 is a block diagram of an example of a system-on-chip integrated circuit 70 that includes a touch screen interface circuit 100 in accordance with a preferred embodiment of the present invention. The integrated circuit 70 includes a plurality of devices that are disposed on a peripheral bus 72 including one or more universal asynchronous receiver-transmitters (UARTs) 73, one or more serial interfaces 74 for interfacing to external devices (such as digital to analog converters (DACs), audio controllers, and so on), interrupt controller/timers 75, a keypad interface 76, one or more I/O ports 77, and a touch screen interface circuit 100 (described in greater detail below). The integrated circuit 70 also includes a plurality of devices that are disposed on a processor bus 80 including one or more universal serial

B/  
Cont

BI  
concl'd  
bus (USB) host interfaces 81 for connection to USB devices such as a keyboard,  
mouse, printer, and so on, an Ethernet port 82, DMA controllers 83, a microprocessor  
86, a display interface 87 (for example, a raster engine), memory controllers 88 and  
90, and boot ROM 89 for storing program code executed during a boot-up sequence.

---

Respectfully submitted,

Date

1/2/03

By

D. Luetzgen

FOLEY & LARDNER  
Suite 3800  
777 East Wisconsin Avenue  
Milwaukee, Wisconsin 53202-5306  
Telephone: (414) 297-5769  
Facsimile: (414) 297-4900

David G. Luetzgen  
Attorney for Applicant  
Registration No. 39,282